REMARKS

Applicant respectfully requests reconsideration of this application as amended. Claims 1-17, 24-26, 41 and 49 have been canceled without prejudice, claims 18, 21, 23, 27, 35, 42, 48 and 50 have been amended and new claims 52-57 have been added. No new matter has been added. Claims 18-23, 27-40, 42-48 and 50-57 are presented for examination. The remarks below refer to the claims as amended herein.

Claim Rejections – 35 U.S.C. § 102

Claims 1-17 and 24-51 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,602,770 to Ohira ("Ohira"). Applicant has canceled claims 1-17, 24-26, 41 and 49 without acquiescence to the reasons for rejection, rendering the rejection of those claims moot. Applicant submits that claims 18-23, 27-40, 42-48, 50 and 51 each include one or more limitations not disclosed by Ohira.

Regarding claim 27, applicant submits that Ohira does not disclose or suggest the following combination:

> a plurality of pairs of group bit lines, each pair of group bit lines being coupled to the plurality of CAM cells of a respective one of the CAM cell groups;
>
> a plurality of group sense amplifiers coupled respectively to the plurality of pairs of group bit lines; and
>
> at least one compare line coupled to the plurality of CAM cells in each of the plurality of CAM cell groups

Ohira discloses an associative memory device having pairs of data lines that are driven by both retrieval data and read/write data (Ohira, col., 11, lines 26-58). Thus, Ohira does not disclose an arrangement having both bit lines and a compare line, much less a compare line that is coupled to a plurality of CAM cells in each of a plurality of CAM cell groups, as recited in claim 27. Because Ohira does not disclose the above recited combination, Ohira does not anticipate claim 27, nor claims 28-34 which depend from and further limit claim 27.

Claim 35 recites, in part:

> switchably forming a path between the first bit line and a second bit line to reduce a voltage of the second bit line to a third level

Ohira discloses an associative memory device having memory cells arranged in columns and rows, with all the memory cells in each column coupled to a corresponding pair of data lines (Ohira, col., 8, lines 4-18). Assuming *arguendo* that the data lines of Ohira constitute bit lines, Ohira does not disclose or suggest switchably forming a path between a first bit line and a second bit line to reduce a voltage of the second bit line to a third level. Thus, Ohira lacks at least the above-recited limitation of claim 35 and therefore does not anticipate claim 35, nor claims 36-40 and 42 which depend from and further limit claim 35.

Claim 43 recites in part:

> enabling a write driver to draw current from a first bit line to reduce a voltage of the first bit line from a precharged level to a first reduced level;
>
> enabling a sense amplifier to draw current from the first bit line to reduce the voltage of the first bit line from the first reduced level to a second reduced level; and
>
> switchably forming a path between the first bit line and a static storage circuit of a CAM cell to enable the second reduced level of the first bit line to switch the static storage circuit from a first state to a second state

Applicant submits that Ohira does not disclose or suggest the above-recited combination and notes that no such disclosure been pointed out. Accordingly, applicant submits that claim Ohira does not anticipate claim 43 nor claims 44-47 which depend from and further limit claim 43.

Claim 48 recites in part:

> means for switchably forming a path between the first bit line and a second bit line to reduce a voltage of the second bit line to a third level

Applicant submits that, at least for the reasons given with respect to claim 35, Ohira does not disclose or suggest the above-recited limitation and, therefore, that Ohira does not anticipate claim 48, nor claim 50 which depends from and further limits claim 48.

Claim 51 recites in part:

> write driver means for drawing current from the first bit line during a first

interval to reduce a voltage of the first bit line to a first reduced level;

sense amplifier means for drawing current from the first bit line during a second interval to reduce the voltage of the first bit line to a second reduced level, the second interval beginning after the first interval and being at least partially encompassed by the first interval

Ohira does not disclose or suggest the above-recited combination and therefore does not anticipate claim 51.

Claim Rejections – 35 U.S.C. § 103(a)

Claims 18-23 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohira in view of U.S. Patent No. 5,936,873 to Kongetira ("Kongetira"). Applicant respectfully submits that claims 18-23 are not anticipated by Kongetira.

Claim 18 recites in part:

a first transistor coupled to form a conductive path between a first bit line of the first pair of bit lines and a first bit line of the second pair of bit lines

As discussed above, Ohira discloses an associative memory device having memory cells arranged in columns and rows, with all the memory cells in each column coupled to a corresponding pair of data lines (Ohira, col., 8, lines 4-18). Assuming *arguendo* that the data lines of Ohira constitute bit lines, Ohira does not disclose or suggest a transistor coupled to form a conductive path between a first bit line of a first pair of bit lines and a second bit line of a second pair of bit lines as recited in applicant's claim 18. Kongetira discloses a translation lookaside buffer having minor and major sense lines (Kongetira, col., 6, lines 21-32), but does not disclose or suggest the above-recited feature (referring to Figure 4 of Kongetira, for example, transistor 320 is not coupled to form a conductive path between lines 230(1)and 296(1)). Accordingly, even if Ohira and Kongetira could be combined in the manner suggested in the Office Action, the combination would still lack at least the above-recited limitation and therefore would not have rendered claim 18 obvious. Because claims 19-23 depend from and further limit claim 18, claims 19-23 also are not obvious in view of the proposed combination.

New Claims

Applicant submits that each of new claims 52-57 includes one or more limitations not

disclosed in Ohira or Kongetira. For example, neither Ohira nor Kongetira discloses the following limitation recited in claim 52:

> a third pair of bit lines coupled to the first pair of bit lines via a first pair of access transistors and to the second pair of bit lines via a second pair of access transistors

Conclusion

Applicant respectfully submits that all pending claims are in condition for allowance. If a telephone interview would be helpful in any way, the examiner is invited to call the undersigned attorney.

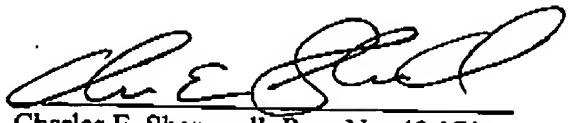
A petition for a one (1) month extension of time is enclosed.

Authorization is hereby given to charge deposit account 501914 for any fee deficiency associated with this Amendment.

Respectfully submitted,

SHEMWELL GREGORY & COURTNEY LLP

Date September 6, 2005



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